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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,313	01/18/2002	Robert L. Hodges	10004054 -1	8400

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EXAMINER	
LEE, HSIEN MING	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 10/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,313	HODGES ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- Th MAILING DATE of this communication appears on the cov r sheet with th corr spond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-13 and 19-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-13 and 19-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Remarks

1. Applicants' cancellation to claims 1-6 and 14-18 is acknowledged. Claims 22-33 are newly added. Claims 7-13 and 19-33 are pending in the application.

2. The objections to specification, drawing and claims 3 and 6; 102(e) rejection to claims 1-6; and 103(a) rejection to claims 14-18 are withdrawn in response to applicants' amendment filed 7/31/03.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 19-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Slater et al. (US 6,344,663~~01~~).

In re claim 19, Slater et al., in Figs. 4-8 and related text teach the claimed method of manufacturing a semiconductor device, comprising:

- depositing a current prevention layer 58 (i.e. a silicon dioxide, col. 11, line 6) proximate a first surface of a semiconductor substrate (Fig.8); and
- forming first 36/54/50/56/38 and second 48/55/52/57/46 field effect transistors (FETs), wherein each said FET includes a gate electrode with associated active areas formed in the first surface of the semiconductor substrate (i.e. 36/54/50/56/38 having

an electrode 50 and active areas 36 and 38 in the substrate; and 48/55/52/57/46 having an electrode 52 and active areas 48 and 46 in the substrate, Fig.8) having the deposited current prevention layer 58 (i.e. a silicon dioxide);

wherein the current prevention layer 58 includes a region that minimizes current flow between the active areas 36 and 38 of the first FET 36/54/50/56/38 with respect to the active areas 48 and 46 of the second FET 48/55/52/57/46 because the silicon dioxide layer 58, including the region between the first and second FETs, serves as an electrical isolation region (Fig.8 and col. 7, lines 36-42).

In re claims 20-21, Slater et al. also teach that the current prevention layer 58 is silicon dioxide (col. 11, line 6), which is a dielectric and an oxide.

(NOTE) The claim body of claim 19 full and intrinsically sets forth all of the limitations of the claimed invention, and the permeable (i.e. manufacturing a fluid ejection device) merely states the purpose of the claimed invention, then the preamble is **not** considered a limitation and is of **no** significant to claims construction. See M.P.E.P. 2111.02

Thus, even Slater et al. do not teach the method is for manufacturing the fluid ejection device, the teachings still reads on claims 19-21 for the aforementioned reasons.

In re claim 22, Slater et al., in Figs. 4-8 and related text teach the claimed method of manufacturing a semiconductor device, comprising:

- depositing a layer of oxide 58 proximate a first surface of a semiconductor substrate (Fig.8);

- exposing a portion of the first surface of the semiconductor substrate, i.e. exposing the portions where transistors (i.e. a first field effect transistor 36/54/50/56/38 and a second field effect transistor 48/55/52/57/46) to be formed; and
- forming a field effect transistor (FET) 36/54/50/56/38 on the exposed portion of the first surface of the substrate having the deposited oxide layer 58, wherein the FET includes a gate electrode 50 with associated active areas 36 and 38 formed in the first surface of the semiconductor substrate.

In re claim 23, Slater et al. also teach a product (i.e. FET) formed by the aforementioned method as recited in claim 22.

In re claim 24, Slater et al., in Figs. 4-9 and related text, also teach the claimed method of making a semiconductor device comprising:

- depositing a layer of oxide 58 proximate a first surface of a semiconductor substrate (Fig.8);
- exposing a portion of the first surface of the semiconductor substrate, i.e. exposing the portions where transistors (i.e. a first field effect transistor 36/54/50/56/38 and a second field effect transistor 48/55/52/57/46) to be formed;
- forming a gate oxide layer 49 on the exposed portion of the first surface, adjacent to the deposited oxide layer 58 (Fig.8);
- forming a pair of active areas 36 and 38 in the exposed portion of the first surface, adjacent the deposited oxide layer 58 and gate oxide layer 49 (Fig.8);
- forming a gate electrode 50 by depositing a conductive layer over the gate oxide layer 49 (Fig.8);

- depositing a dielectric layer 60 (i.e. a protection layer) over the gate electrode 50, active areas 36 and 38, and deposited oxide layer 58 (Fig.9); and
- forming electrical contacts 59 to the pair of active areas 36 and 38 and the gate electrode 50.

5. Claims 24-33 is rejected under 35 U.S.C. 102(e) as being anticipated by Hiroki et al. (US 6,485,132).

In re claims 24 and 27, Hiroki et al., in Fig.4 and related text, teach the claimed method of making a semiconductor device comprising:

- depositing a layer of oxide 416 proximate a first surface of a semiconductor substrate;
- exposing a portion of the first surface of the semiconductor substrate, exposing the portions where transistors 450 and 451to be formed;
- forming a gate oxide layer 408 on the exposed portion of the first surface, adjacent to the deposited oxide layer 416;
- forming a pair of active areas 405 and 406 in the exposed portion of the first surface, adjacent the deposited oxide layer 416 and gate oxide layer 408, wherein the active areas 405 and 406 are formed by impurity implant and diffusion (col. 9, lines 2-3);
- forming a gate electrode 415 by depositing a conductive layer over the gate oxide layer 408;
- depositing a dielectric layer 418 over the gate electrode 415, active areas 405 and 406, and deposited oxide layer 416; and
- forming electrical contacts 417 to the pair of active areas 405 and 406 and the gate electrode 415 via the active areas 405 and 406.

In re claims 25 and 26, Hiroki et al. also teach thermally growing a thermal oxide layer 453 before depositing the layer of oxide 416 on the first surface of the semiconductor substrate, wherein the substrate is P type silicon (col. 8, line 66).

In re claim 28, Hiroki et al. also teach that the active areas 405 and 406 are n doped regions (col. 9, lines 2-3).

In re claim 29, Hiroki et al. also teach that the conductive layer 415 over the gate oxide layer 408 is polysilicon (col. 9, lines 2-4).

In re claim 30, Hiroki et al. also teach that the dielectric layer 418 is silicon dioxide (col. 9, lines 28-29).

Although it is noted that claims 31-33 are a product-by-process claim, product-by-process claims are directed to the product no matter how actually made. *In re Taylor*, 149 USPQ 615, 617 (CCPA 1966). Consequently, it is the patentability of the **final product**, and **not** the patentability of the process, that must be determined in a product-by-process claim. *In re Thorpe*, 227 USPQ 964, 966 (CAFC 1985), *Ex parte Edwards* 231 USPQ 981, 983 (BdPatApp&Int 1986).

In re claims 31-33, Hiroki et al. teach the claimed fluid ejection device or a semiconductor device produced by a method (Fig.4), comprising:

- forming a first (i.e. drain region 406 of p-MOS 450) and second (i.e. source region 405 of n-MOS 451) active areas in a first surface of a semiconductor substrate 401;
- depositing a current prevention layer 416 (i.e. a silicon oxide layer) on the first surface in between the first (i.e. 406 of 450) and second (i.e. 405 of 451) active areas;

- forming a gate oxide 408 on the first surface adjacent to the second active area (i.e. 405 of 451); and
- forming a gate electrode 415 for a driver transistor 451 (i.e. the n-MOS is used for driving purpose, col. 9, lines 9-10) of the fluid ejection device on the gate oxide 408, wherein the current prevention layer 416 minimizes current flow between the first and second active areas and the gate electrode 415 because the current prevention layer 416 is a dielectric layer.

6. Claims 7, 9-13 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Gardner (US 6,200,862).

In re claims 7, 9, and 12, Gardner et al. teach the claimed method (Fig. 2A-2C), comprising:

- depositing a layer of oxide 40 proximate a first surface of a semiconductor substrate 10 (p-type silicon, col.3, lines 24-31);
- forming a gate oxide layer 22 on the first surface, adjacent to the deposited oxide layer 40;
- forming a pair of active areas 28/34 in the first surface, adjacent to the deposited oxide layer 40 and gate oxide layer 22 (Fig.2B);
- forming a gate electrode 24 by depositing a conductive layer (polysilicon, col.3, lines 57-58) over the gate oxide layer 22 (Fig.2A);
- depositing a dielectric layer 46 over the gate electrode 24,active region 28/34, and deposited oxide layer 40 (Fig.2C); and
- forming electrical contacts 44 to the pairs of active areas 28/34 and the gate electrode 24.

In re claim 10, Gardner et al. also teach that the active areas 28/34 are formed by impurity implant and diffusion, i.e. forming source/drains (col.4, 5-30).

In re claim 11, Gardner et al. also teach that the active areas 28/34 are n-doped regions when channel is p-type (col. 3, lines 30-31 and col.4, lines 2-5).

In re claim 13, Gardner et al. also teach that the dielectric layer 46 is silicon dioxide (col. 4, lines 62-63).

In re claim 32, Gardner et al. also teach a semiconductor device (i.e. a insulated gate transistor or IGFET) produced by the method of claim 7.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (US '862) in view of Liu et al. (US 2003/0081070).

Gardner et al. teach all limitations, as stated above, but do not teach thermally growing a thermal oxide layer before depositing the layer of oxide on the first surface of the semiconductor substrate.

However, Liu et al., in an analogous art, teach thermally growing a thermal oxide layer 32 before depositing the layer of oxide 36 on the first surface of the semiconductor substrate 25 (Figs 3A-3B).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to thermally grow the oxide, as taught by Liu et al, before depositing the oxide layer of Gardner et al., since by doing so it would provide a better electrical insulation for adjacent layers.

Response to Arguments

9. Applicant's arguments filed 7/31/03 have been fully considered but they are not persuasive.

In re claims **7 and 9-13**, applicants argue that Gardner et al. fail to teach or suggest depositing a layer of oxide proximate a first surface of a semiconductor substrate. (second and third paragraphs, page 11)

Contrary to the argument, Gardner et al. in Fig. 2A-2C and col. 4, lines 40-42, explicitly teach depositing a layer of oxide 40 (i.e. silicon oxide) proximate a first surface of a semiconductor substrate 10, i.e. depositing the silicon oxide adjacent to a top surface of the substrate 10, as illustrated in Fig.2C.

Applicants also assert that column 4, lines 24-31 of Gardner et al. only provide information related to the substrate, not related to the deposition of the oxide as recited in claim 7. (third paragraph, page 11)

In response to the argument, the teachings stated in col. 3, lines 30-31, i.e. "[t]he substrate can be doped with boron ions to form a p-doped channel (or p-channel) regions", is to reject claim 9 because the substrate of Gardner et al. is p-type silicon (i.e. silicon substrate doped with boron).

For these reasons, the 102(e) rejection to claims 7 and 9-13 as set forth in the previous Office Action is deemed proper.

In re claims **19-21**, applicants argue that Hiroki et al. fail or suggest the claimed invention because the interlayer insulation layer 416 of Hiroki et al. is formed after each of the elements is formed. (third paragraph, page 12).

In response to the argument, the claimed invention merely recites " depositing a current prevention layer proximate a first surface of a semiconductor substrate" and "said FETs includes a gate electrode ... in the first surface of the semiconductor substrate having the deposited current prevention layer." It does not claim either forming the current prevention layer **before** any elements are formed or **after** any elements are formed. Thus, the aforementioned argument is no the issue.

In addition, the arguments with respect to claims 19-21 are moot in view of the new ground(s) of rejection in response to applicants' amendment.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien-Ming Lee
Examiner
Art Unit 2823

Oct. 28,2003